IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLN. OF:

FURUMIYA et al.

FILED:

October 17, 2003

FOR:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

DOCKET:

NEC 03FN026

MAIL STOP PATENT APPLICATION Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In connection with the above-entitled matter, Applicants hereby attach U.S. Patent Office Form PTO-1449, including copies of the references listed therein, which were considered prior to the initial filing, and are discussed in the specification. The claims in the present application are believed to be patentably distinguished over these references.

This information disclosure statement is being made pursuant to the duty of disclosure imposed by law and formulated in 37 CFR 1.56(A). No representation is made that the information thus disclosed in fact constitutes prior art or that it is the closest prior art, inasmuch as 37 CFR 1.56(A) relies on a materiality concept which depends on subjectivity.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account No. 08-1391.

Respectfully submitted,

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Docket Number (Optional) Application Number **NEC 03FN026** INFORMATION DISCLOSURE CITATION Applicant(s) FURUMIYA et al. (Use several sheets if necessary) Filing Date Group Art Unit October 17, 2003 **U.S. PATENT DOCUMENTS** EXAMINER FILING DATE REF DOCUMENT NUMBER DATE NAME CLASS SUBCLASS INITIAL IF APPROPRIATE FOREIGN PATENT DOCUMENTS Translation DOCUMENT NUMBER DATE REF COUNTRY **CLASS** SUBCLASS YES NO 16.01.1998 H01L 27/04 10-012825 JAPAN (w/Abstract) 2002-124636 26.04.2002 JAPAN (w/Abstract) H01L 27/04 OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER

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